Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. Please enter new claims 21-48.

Listing of Claims:

1. (currently amended) A method for making a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a trench within the first dielectric layer, wherein the trench is formed by removing a mask layer and a polysilicon layer, and wherein the mask layer protects the polysilicon layer during a silicide process;

forming a second dielectric layer on the substrate, the second dielectric layer having a first part that is formed at the bottom of the trench and a second part;

forming a first metal layer on the first part of the second dielectric layer but not covering the second part of the second dielectric layer; and

forming a second metal layer on the first metal layer and on the second part of the second dielectric layer, the second metal layer covering the first metal layer and covering the second part of the second dielectric layer.

2. (original) The method of claim 1 wherein the second dielectric layer comprises a high-k gate dielectric layer.

3. (original) The method of claim 2 wherein the high-k gate dielectric layer comprises a material that is selected form the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

4. (original) The method of claim 1 wherein the first metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer comprises a material that is selected form the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

5. (original) The method of claim 1 wherein the first metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide and the second metal layer comprises a material that is selected form the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide.

6. (original) The method of claim 1 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction

that is between about 3.9 eV and about 4.2 eV, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV.

7. (original) The method of claim 1 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV.

8. (original) The method of claim 1 further comprising forming a fill metal within the trench and on the second metal layer.

9. (original) The method of claim 1 further comprising forming an underlayer metal on the second dielectric layer prior to forming the first metal layer.

10. (original) The method of claim 1 further comprising forming the first metal layer on the first part of the second dielectric layer by forming a metal layer on both the first and second parts of the second dielectric layer, then removing the metal layer from the second part of the dielectric layer.

11. (original) The method of claim 10 wherein the first metal layer is formed on the first part of the second dielectric layer by:

forming a metal layer on both the first and second parts of the second dielectric layer;

forming a spin on glass layer on the metal layer, a first part of the spin on glass layer covering the first part of the second dielectric layer and a second part of the spin on glass layer covering a second part of the second dielectric layer;

removing the second part of the spin on glass layer while retaining the first part of the spin on glass layer, exposing part of the metal layer;

removing the exposed part of the metal layer to generate the first metal layer that covers the first part of the second dielectric layer but does not cover the second part of the second dielectric layer; then

removing the first part of the spin on glass layer.

12. (currently amended) A method for making a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a trench within the first dielectric layer;

forming a high-k gate dielectric layer on the substrate, the high-k gate dielectric layer having a first part that is formed at the bottom of the trench and a second part;

forming a metal layer on both the first and second parts of the high-k gate dielectric layer;

forming a spin on glass layer on the metal layer, a first part of the spin on glass layer covering the portion of the metal layer that covers the first part of the high-k gate dielectric layer in the trench and a second part of the spin on glass layer covering the portion of the metal layer that covers the ~~a~~ second part of the high-k gate dielectric layer;

removing the second part of the spin on glass layer while retaining the first part of the spin on glass layer, exposing part of the metal layer;

removing the exposed part of the metal layer to generate a first metal layer that covers the first part of the high-k gate dielectric layer but does not cover the second part of the high-k gate dielectric layer;

removing the first part of the spin on glass layer; and

forming a second metal layer on the first metal layer and on the second part of the high-k gate dielectric layer, the second metal layer covering the first metal layer and covering the second part of the high-k gate dielectric layer.

13. (original) The method of claim 12 wherein the high-k gate dielectric layer comprises a material that is selected form the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

14. (original) The method of claim 12 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer has a workfunction that is between about 4.9

eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and further comprising forming a fill metal within the trench and on the second metal layer.

15. (original) The method of claim 12 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and further comprising forming a fill metal within the trench and on the second metal layer.

16. (currently amended) A method for making a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a trench within the first dielectric layer;

forming a high-k gate dielectric layer on the substrate, the high-k gate dielectric layer having a first part that is formed at the bottom of the trench and a second part, the high-k gate dielectric layer comprising a material that is selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide;

forming a metal layer on both the first and second parts of the high-k gate dielectric layer, the metal layer being between about 25 and about 300 angstroms thick;

forming a spin on glass layer on the metal layer, a first part of the spin on glass layer covering the portion of the metal layer that covers the first part of the high-k gate dielectric layer in the trench and a second part of the spin on glass layer covering the portion of the metal layer that covers the ~~a~~ second part of the high-k gate dielectric layer;

removing the second part of the spin on glass layer while retaining the first part of the spin on glass layer, exposing part of the metal layer;

removing the exposed part of the metal layer to generate a first metal layer that covers the first part of the high-k gate dielectric layer but does not cover the second part of the high-k gate dielectric layer;

removing the first part of the spin on glass layer; and

forming a second metal layer on the first metal layer and on the second part of the high-k gate dielectric layer, the second metal layer being between about 25 and about 300 angstroms thick and covering the first metal layer and the second part of the high-k gate dielectric layer.

17. (original) The method of claim 16 wherein the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

18. (original) The method of claim 16 wherein the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide.

19. (original) The method of claim 16 further comprising forming a fill metal within the trench and on the second metal layer.

20. (original) The method of claim 19 wherein the fill metal comprises a material that is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride.

21. (new) The method of claim 1 wherein the second part of the second dielectric layer is formed at the bottom of the same trench as the first part of the second dielectric layer.

22. (new) The method of claim 21 wherein the semiconductor device comprises a P/N junction at the vertical interface formed where the first metal layer and the second metal layer meet at the bottom of the trench.

23. (new) The method of claim 8 wherein the fill metal is subsequently polished back.

24. (new) The method of claim 1 wherein the first metal layer is formed subsequent to removing impurities from the second dielectric layer and increasing the oxygen content of the second dielectric layer.

25. (new) The method of claim 24 wherein removing impurities from the second dielectric layer and increasing the oxygen content of the second dielectric layer comprise exposing the second dielectric layer to an aqueous solution that contains between about 2% and about 30% hydrogen peroxide by volume between about 15°C and about 40°C for at least about 1 minute.

26. (new) The method of claim 12 wherein the second part of the high-k gate dielectric layer is formed at the bottom of the same trench as the first part of the high-k gate dielectric layer.

27. (new) The method of claim 26 wherein the semiconductor device comprises a P/N junction at the vertical interface formed where the first metal layer and the second metal layer meet at the bottom of the trench.

28. (new) The method of claim 14 wherein the fill metal is subsequently polished back.

29. (new) The method of claim 15 wherein the fill metal is subsequently polished back.

30. (new) The method of claim 13 wherein the first metal layer is formed subsequent to removing impurities from the high-k gate dielectric layer.

31. (new) The method of claim 13 wherein the first metal layer is formed subsequent to increasing the oxygen content of the high-k gate dielectric layer.

32. (new) The method of claim 16 wherein the second part of the high-k gate dielectric layer is formed at the bottom of the same trench as the first part of the high-k gate dielectric layer.

33. (new) The method of claim 16 wherein the semiconductor device comprises a P/N junction at the vertical interface formed where the first metal layer and the second metal layer meet at the bottom of the trench.

34. (new) The method of claim 20 wherein the fill metal is subsequently polished back.

35. (new) The method of claim 16 wherein the first metal layer is formed subsequent to removing impurities from the high-k gate dielectric layer.

36. (new) A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate; and

subsequent to forming said dielectric layer, forming a trench within said dielectric layer, wherein said trench is formed by removing a mask layer and a polysilicon layer, and wherein said mask layer protects said polysilicon layer during a previous silicide process; and

subsequent to forming said trench, forming a high-k gate dielectric layer on said substrate, said high-k gate dielectric layer having a first part that is formed at the bottom of said trench and a second part; and

subsequent to forming said high-k gate dielectric layer, forming a first metal layer on said first part of said high-k gate dielectric layer but not covering said second part of said high-k gate dielectric layer; and

subsequent to forming said first metal layer, forming a second metal layer on said first metal layer and on said second part of said high-k gate dielectric layer, wherein said second metal layer comprises a different material than said first metal layer.

37. (new) The method of claim 36 wherein said second part of said high-k gate dielectric layer is formed at the bottom of said trench, and wherein said semiconductor device comprises a P/N junction at the vertical interface formed where said first metal layer and said second metal layer meet at the bottom of said trench.

38. (new) The method of claim 36 wherein patterning said first metal layer comprises using a spin on glass layer.

39. (new) The method of claim 36 wherein said first metal layer is formed subsequent to removing impurities from said high-k gate dielectric layer and increasing the oxygen content of said high-k gate dielectric layer, wherein removing impurities from said high-k gate dielectric layer and increasing the oxygen content of said high-k gate dielectric layer comprise exposing said high-k gate dielectric layer to an aqueous solution that contains between about 2% and about 30% hydrogen peroxide by volume between about 15°C and about 40°C for at least about 1 minute.

40. (new) A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate; and

subsequent to forming said dielectric layer, forming a trench within said dielectric layer; and

subsequent to forming said trench, forming a high-k gate dielectric layer on said substrate, said high-k gate dielectric layer having a first part that is formed at the bottom of said trench and a second part that is formed at the bottom of said trench; and

subsequent to forming said high-k gate dielectric layer, forming a first metal layer on said first part of said high-k gate dielectric layer but not covering said second part of said high-k gate dielectric layer; and

subsequent to forming said first metal layer, forming a second metal layer on said first metal layer and on said second part of said high-k gate dielectric layer,

wherein said second metal layer comprises a different material than said first metal layer.

41. (new) The method of claim 40 wherein said semiconductor device comprises a P/N junction at the vertical interface formed where said first metal layer and said second metal layer meet at the bottom of said trench.

42. (new) The method of claim 40 wherein said high-k gate dielectric layer comprises a material that is selected form the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

43. (new) The method of claim 42 wherein said first metal layer is formed subsequent to removing impurities from said high-k gate dielectric layer and increasing the oxygen content of said high-k gate dielectric layer, wherein removing impurities from said high-k gate dielectric layer and increasing the oxygen content of said high-k gate dielectric layer comprise exposing said high-k gate dielectric layer to an aqueous solution that contains between about 2% and about 30% hydrogen peroxide by volume between about 15°C and about 40°C for at least about 1 minute.

44. (new) A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a first trench and a second trench within said dielectric layer;

forming a first metal layer at the bottom of said first trench and at the bottom of said second trench;

forming a spin on glass layer on said first metal layer at the bottom of said first trench and said second trench;

removing the portion of said spin on glass layer that covers said first metal layer in said second trench to expose the portion of said first metal layer at the bottom of said second trench and to retain the portion of said spin on glass layer that covers said first metal layer in said first trench;

removing the exposed portion of said first metal layer from the bottom of said second trench;

removing the portion of said spin on glass layer that covers said first metal layer in said first trench to expose the portion of said first metal layer at the bottom of said first trench; and

forming a second metal layer at the bottom of said second trench and on said first metal layer at the bottom of said first trench, wherein said second metal layer comprises a different material than said first metal layer.

45. (new) The method of claim 44 further comprising forming a fill metal within said first and said second trench and on said second metal layer, wherein said fill metal comprises

a material that is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride, and wherein said fill metal is subsequently polished back.

46. (new) A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a trench within said dielectric layer;

forming a first metal layer at the bottom of said trench;

forming a spin on glass layer on said first metal layer at the bottom of said trench;

removing a portion of said spin on glass layer so as to leave covered a first portion of said first metal layer at the bottom of said trench and to expose a second portion of said first metal layer in said trench;

removing said second portion of said first metal layer from the bottom of said trench to expose a portion of the bottom of said trench;

removing the portion of said spin on glass layer that covers said first portion of said first metal layer in said trench to expose said first portion of said first metal layer at the bottom of said trench; and

forming a second metal layer that covers said portion of the bottom of said trench and said first portion of said first metal layer at the bottom of said trench, wherein said second metal layer comprises a different material than said first metal layer.

47. (new) The method of claim 46 wherein said semiconductor device comprises a P/N junction at the vertical interface formed where said first metal layer and said second metal layer meet at the bottom of said trench.

48. (new) The method of claim 46 further comprising forming a fill metal within said trench and on said second metal layer, wherein said fill metal comprises a material that is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride, and wherein said fill metal is subsequently polished back.